

CLAIMS

5 *Sale* 1. A microcomputer including a read-only memory that stores programs, a controller/calculator that successively accesses to addresses of the programs stored in said read-only memory to retrieve and decode an instruction from each of the accessed addresses, thereby executing a processing based on the decoded instruction, and a program counter in which an address to be accessed by said controller/calculator is 10 successively renewed and indicated, said microcomputer comprising:

at least one comparison-address-storage device that stores a comparison address data corresponding to an optional address of the programs stored in said read-only memory, at 15 which an interruption-processing should be executed to virtually revise the programs stored in said read-only memory; a random-access memory that stores a revisional program in which said interruption-processing is programmed;

20 at least one vector-address-storage device that stores a vector address data corresponding to a head address of said revisional program stored in said random-access memory; and an address comparator that compares said comparison address data with an address successively renewed in said program counter,

25 wherein said controller/calculator makes an access to

the head address of said revisional program, stored in said random-access memory, corresponding to said vector address data stored in said vector-address-storage device, when it is determined by said address comparator that there is a coincidence between said comparison address data and the renewed address of said program counter, resulting in an execution of said interruption-processing in accordance with said revisional program.

2. A microcomputer as set forth in claim 1, further comprising:

a discrimination system that discriminates whether the coincidence between said comparison address data and the renewed address of said program counter is proper; and
an address-coincidence-disabling system that disables the coincidence between said comparison address data and the renewed address of said program counter.

3. A microcomputer as set forth in claim 1, further comprising:

a rewritable and non-volatile memory that stores said revisional program, said comparison address data and said vector address data;

a reading/writing system that reads said revisional program, said comparison address data and said vector address data from said rewritable and non-volatile memory, and then writes these data in said random-access memory, said

comparison-address-storage device and said vector-address-storage device, respectively, whenever the microcomputer is powered ON.

4. A microcomputer as set forth in claim 1, wherein
5 said address comparator is connected to said program counter to thereby retrieve the renewed address therefrom.

5. A microcomputer as set forth in claim 1, wherein
said address comparator is connected to an address bus
extending to said program counter, to thereby retrieve the
10 renewed address therefrom.

6. A microcomputer as set forth in claim 1, further comprising a vector-address data setting system that reads the vector address data from said vector-address-storage device, and is then set in said program counter, whereby the access to the head address of said revisional program by said controller/calculator is made, resulting in the execution of said interruption-processing in accordance with said revisional program.

7. A microcomputer as set forth in claim 1, further
20 comprising:

a vector-address-temporary-storage device that receives the vector address data from said vector-address-storage device, when it is determined by said address comparator that there is the coincidence between said comparison address data and the renewed address of said program counter; and

a vector-address data setting system that reads the
vector address data from said vector-address-temporary-storage
device, and is then set in said program counter, whereby the
access to the head address of said revisional program by said
controller/calculator is made, resulting in the execution of
5 said interruption-processing in accordance with said
revisional program.

8. A microcomputer as set forth in claim 1, further
comprising:

10 a return-address-setting system that sets said
comparison address data as a return-address data in said
program counter when the execution of said interruption-
processing in accordance with said revisional program is
completed; and

15 an address-coincidence-disabling system that disables
the coincidence between said comparison address data and said
return-address set in said program counter by said return-
address-setting system.